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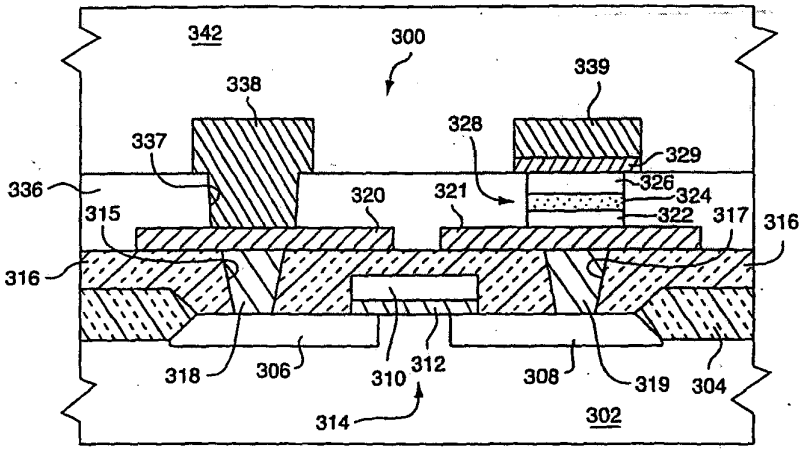

(57) Abstract

A diffusion barrier layer (130, 136, 329, 320, 321, 630) in an integrated circuit is located to inhibit undesired diffusion of chemical species from local interconnects (158, 318, 319, 339, 658) into layered superlattice material in a thin film (124, 324, 624) memorycapacitor (128, 328, 600). The diffusion barrier layer comprises iridium oxide. The thinfilm of layered superlattice material is ferroelectric or nonferroelectric, high-dielectric constant material. Preferably, the thin film comprises ferroelectric layered superlattice material. The diffusion barrier layer is located between a local interconnect and the memory capacitor. Preferably, the diffusion barrier layer is in direct contact with the local interconnect. The iridium-oxide diffusion barrier is effective for preventing diffusion of metals, silicon and other chemical species.

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IRIDIUM OXIDE DIFFUSION BARRIER BETWEEN LOCAL INTERCONNECT LAYER AND THIN FILM OF LAYERED SUPERLATTICE MATERIAL

BACKGROUND OF THE INVENTION

1. *Field of the Invention*

The invention relates to a composition of material used in an integrated circuit that protects electronic properties of memory capacitors by inhibiting diffusion of metals from local interconnects into layered superlattice material oxides.

2. *Statement of the Problem*

Layered superlattice materials contained in memory capacitors of a nonvolatile, ferroelectric random access memory cell ("FeRAM") are metal-oxide compounds. A ferroelectric capacitor is useful in a nonvolatile memory cell when it possesses desired electronic characteristics, such as high residual polarization, good coercive field, high fatigue resistance, and low leakage current. Layered superlattice material oxides possess favorable characteristics for use in nonvolatile integrated circuit memories. See Watanabe, U.S. Patent No. 5,434,102. Certain nonferroelectric layered superlattice materials are useful in dynamic random access memory ("DRAM") cells because they exhibit high dielectric constants.

A typical memory in an integrated circuit contains a semiconductor substrate and a metal-oxide semiconductor field-effect transistor (MOSFET) in electrical contact with a ferroelectric or dielectric device, usually a capacitor. A memory capacitor typically contains a thin film of ferroelectric or dielectric material located between a first or bottom electrode and a second or top electrode, the electrodes typically containing platinum.

The most common scheme of local interconnect ("LI") metallization in FeRAM and DRAM cells contains titanium or titanium nitride or both. The electrodes of the memory capacitors typically are platinum metal. During backend processes after formation of the LI, titanium ("Ti") diffuses through the platinum, or other metal, electrode into the thin film of capacitor dielectric, where it displaces certain atoms, for example, tantalum, niobium and zirconium, from their sites in the crystal lattice. The substitution of titanium atoms into the metal-oxide crystal structure degrades the electronic properties of the capacitor. This problem is acute in memories containing layered superlattice material compounds because these oxide compounds are

particularly complex and prone to degradation by titanium.

A LI layer typically contains other chemical species besides titanium that are capable of diffusing through platinum electrode layers or other types of electrode layers, causing damage to the layered superlattice material. Examples of such other chemical species are: aluminum, copper, titanium, titanium nitride and tungsten. Tungsten and polycrystalline silicon are typically contained in LI plugs providing electrical contact between a MOSFET and a memory capacitor. Tungsten and silicon are able to diffuse through an electrode and damage layered superlattice material.

Integrated circuit devices containing thin films of layered superlattice materials are currently being manufactured. Nevertheless, the problem of diffusion of titanium and other chemical species out of the LI layers into the layered superlattice material, and the resulting degradation of electronic properties during the manufacturing process, hinders the economical production in commercial quantities of FeRAMs, DRAMs, and other IC devices of good quality using the layered superlattice material compounds. There is a need for barrier material that can be incorporated into the integrated circuit between the thin film of layered superlattice material and the LI to prevent diffusion of titanium and other chemical species into the layered superlattice material. The barrier material must remain a good electrical conductor, as well as a diffusion barrier, at the moderately high temperatures, for example, at 500°C, at which some backend manufacturing processes are conducted.

In a study by Nakamura et. al., reported in *Jpn. J. of Appl. Phys.*, Vol. 33, 5207-5210 (1994), a 50 nm-thick layer of iridium oxide was used as part of both the bottom and top platinum electrodes in capacitors having a thin film of PZT. The 2Pr-value of about 33 $\mu C/cm^2$ showed virtually no change due to fatigue after 10^{12} bipolar pulses at 5 volts. In PZT capacitors with Pt/Ti electrodes and no iridium or iridium oxide, the 2Pr-value was initially less at about 25 $\mu C/cm^2$, and it decreased about 50% after 10^8 cycles; but the iridium oxide was not disclosed as a barrier to protect layered superlattice material or to inhibit diffusion of chemical species from a local interconnect into the dielectric thin film of a capacitor.

United States Patent Number 5,773,314, issued June 30, 1998 to Jiang et. al., discloses a barrier region and a bottom electrode comprising iridium oxide to protect tungsten plugs by functioning as barriers to oxygen; however, in this reference, the iridium oxide is not disclosed as a barrier to metal diffusion into the dielectric layer of

a capacitor.

3. *Solution to the Problem*

The invention solves the problems discussed above by disclosing a novel composition of material for use as a diffusion barrier to protect layered superlattice material. The inventive composition is iridium oxide ("IrO_2").

A feature of the invention is an integrated circuit in which a diffusion barrier layer comprising iridium oxide is located to inhibit diffusion of titanium and other chemical species towards a thin film of layered superlattice material. The inventive diffusion barrier layer is located between a local interconnect and the thin film of layered superlattice material. Preferably, the diffusion barrier layer is in direct contact with the local interconnect.

In a typical embodiment of the invention, the local interconnect is a metallized wiring layer, and the thin film of layered superlattice material is a dielectric thin film in a memory capacitor. Typically, a metal top electrode layer of a memory capacitor is formed on the dielectric thin film of layered superlattice material, and then the diffusion barrier layer is located on the top electrode layer. The metallized layer is located above the diffusion barrier layer, preferably in direct contact with the diffusion barrier layer. The metallized wiring layer typically contains aluminum, titanium, titanium nitride, copper and tungsten, as well as other metals. The diffusion barrier layer inhibits the diffusion of such metals from the metallized wiring layer towards the dielectric thin film.

In another embodiment of the invention, the local interconnect is an electrically conductive plug that serves to connect a MOSFET of a memory cell to the memory capacitor. The memory capacitor has a bottom electrode, and the diffusion barrier layer is located under the bottom electrode and above the conductive plug. Preferably, the diffusion barrier layer is in direct contact with the plug. The conductive plug typically comprises chemical species including polycrystalline silicon or tungsten, and the diffusion barrier layer inhibits diffusion of the chemical species from the conductive plug towards the dielectric thin film of the memory capacitor.

Preferably, the layered superlattice material is a ferroelectric layered superlattice material. For example, layered superlattice material comprising strontium, bismuth and tantalum ("strontium bismuth tantalate" or "SBT") is an effective dielectric thin film in a FeRAM; SBT having a chemical formula $SrBi_2Ta_2O_9$ is widely used by

those skilled in the art. Another effective ferroelectric layered superlattice material contains strontium, bismuth, tantalum and niobium ("strontium bismuth tantalum niobate" or "SBTN"); SBTN having a chemical formula $SrBi_{2.18}(Ta_{1-x}Nb_x)_2O_9$, where $0<x<1$, is widely used in the art. The layered superlattice material may also be nonferroelectric, high-dielectric constant material.

Another feature of the invention is a method of forming an integrated circuit. In one basic embodiment, the method comprises steps of: forming a thin film of layered superlattice material; forming a local interconnect; and forming a diffusion barrier layer, the diffusion barrier layer comprising iridium oxide and located between the thin film of layered superlattice material and the local interconnect. Typically, the local interconnect is formed as a metallized wiring layer; and the thin film of layered superlattice material is formed as a dielectric thin film in a memory capacitor. The method may further comprise a step of forming a top electrode layer on the dielectric thin film, wherein the diffusion barrier layer is formed on the top electrode layer, and the metallized wiring layer is formed on the diffusion barrier layer.

In another basic embodiment, the local interconnect is formed as an electrically conductive plug, and the thin film of layered superlattice material is formed as a dielectric thin film in a memory capacitor. Typically, the diffusion barrier layer is formed above the electrically conductive plug, a bottom electrode layer is formed on the diffusion barrier layer, and then the thin film of layered superlattice material is formed on the bottom electrode layer.

Numerous other features, objects and advantages of the invention will become apparent from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a portion of an integrated circuit showing a memory cell in which the memory capacitor is displaced laterally from the switch, and a diffusion barrier layer comprising iridium oxide has been patterned with the top electrode layer of the capacitor;

FIG. 2 is a cross-sectional view of a portion of an integrated circuit showing a memory capacitor in which a diffusion barrier layer comprising iridium oxide has been formed in the wiring hole at the top electrode;

FIG. 3 is a cross-sectional view of another embodiment of the invention,

showing a memory cell in which a memory capacitor is stacked substantially above the switch region of the memory cell, and in which diffusion barrier layers comprising iridium oxide are located between the switch region and the overlying region containing the memory capacitor;

FIG. 4 is a flow chart showing the preferred embodiment of a process for fabricating a memory device incorporating a diffusion barrier layer according to the invention, as depicted in FIG. 1;

FIG. 5 is a top view of an exemplary wafer on which thin film capacitors and diffusion barrier layers fabricated in accordance with the invention are shown greatly enlarged;

FIG. 6 is a portion of a cross-section of FIG. 5 taken through the line 6-6, illustrating a thin film capacitor device fabricated in accordance with the invention; and

FIG. 7 is a graph of hysteresis curves measured at 3 volts, in which polarization, $\mu C/cm^2$, is plotted versus annealing temperature, in units of degrees Celsius, in strontium bismuth tantalate thin-film capacitors, to study the effects of diffusion barrier layers comprising iridium oxide, in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

1. Overview and Description of Integrated Circuit

It should be understood that FIGS. 1-3, 5, and 6 depicting ferroelectric integrated circuit devices are not meant to be actual plan or cross-sectional views of any particular portions of actual integrated circuit devices. In actual devices, the layers will not be as regular and the thicknesses may have different proportions. The various layers in actual devices often are curved and possess overlapping edges. The figures instead show idealized representations that are employed to depict more clearly and fully the structure of the invention than would otherwise be possible.

Also, the figures represent only several of innumerable variations of ferroelectric or nonferroelectric, high-dielectric constant devices that could be fabricated using the method of the invention. FIGS. 1-2 depict ferroelectric memories containing a switch in the form of a field effect transistor in electrical connection with a ferroelectric capacitor displaced laterally from the switch. But, as depicted in FIG. 3, it is also contemplated to use the invention in a FeRAM or DRAM containing a stacked capacitor connected via a plug to the switch element below the capacitor. The invention can also be applied in a FET memory in which the ferroelectric element

is incorporated in the switch element. Such a ferroelectric FET was described in McMillan, U.S. Patent No. 5,523,964. Likewise, other integrated circuits fabricated using the unique diffusion barrier layers of the invention could include other elements and compositions of material. For example, although this description of the invention focuses on a diffusion barrier layer used to protect a ferroelectric nonvolatile memory, the invention is useful to protect integrated circuit devices containing nonferroelectric, high-dielectric constant layered superlattice materials against damage caused by diffusion of chemical species contained in local interconnects.

Since ferroelectric material used in integrated circuits also possesses dielectric properties, the term "dielectric" is used in some places of this disclosure to refer generally both to structures or materials having ferroelectric properties and to those with nonferroelectric, high-dielectric constant characteristics. If the meaning is not clear from the context, the broader definition that includes both ferroelectric and nonferroelectric, high-dielectric constant materials should be used.

A material is considered to have a "high" dielectric constant if its dielectric constant is 20 or higher. Where high-dielectric constant materials are used, it is usually preferred that the dielectric constant be 50 or higher.

In FIG. 1, there is shown a cross-sectional view of an exemplary nonvolatile ferroelectric memory cell 100 that could be fabricated according to the invention. The general manufacturing steps for fabricating integrated circuits containing MOSFETs and ferroelectric capacitor elements are described in U.S. Patent No. 5,466,629 issued November 14, 1995, to Mihara et al., and U.S. Patent No. 5,468,684 issued November 21, 1995, to Yoshimori et al. General fabrication methods have been described in other references also. Therefore, the elements of the circuit of FIG. 1 will be simply identified here. For the sake of clarity, identical elements depicted in FIGS. 1 and 2 are identified with the same reference numerals.

In FIG. 1, a field oxide region 104 is formed on a surface of a silicon substrate 102. A source region 106 and a drain region 108 are formed separately from each other within silicon substrate 102. A gate insulating layer 110 is formed on the silicon substrate 102 between the source and drain regions 106 and 108. Further, a gate electrode 112 is formed on the gate insulating layer 110. These source region 106, drain region 108, gate insulating layer 110 and gate electrode 112 together form a MOSFET 114.

A first interlayer dielectric layer (ILD) 116 made of BPSG (boron-doped phospho-silicate glass) is formed on substrate 102 and field oxide region 104. An adhesion layer 118 is formed on ILD 116. The adhesion layer 118 is made of, for example, titanium, and typically has a thickness of 20 nm. Adhesion layers, such as titanium, enhance the adhesion of the electrodes to adjacent underlying or overlying layers of the circuits.

As depicted in FIG. 1, a bottom electrode layer 122 made of platinum and having a thickness of 200 nm is deposited on adhesion layer 118. The titanium in adhesion layer 118 is typically stabilized by oxidation; therefore, it does not diffuse upwards through bottom electrode layer 122. A dielectric thin film 124 of ferroelectric layered superlattice material is formed on bottom electrode layer 122. A top electrode layer 126, made of platinum and having a thickness of 200 nm, is formed on the thin film 124 of layered superlattice material. Electrode layers 122 and 126 together with thin film 124 of layered superlattice material form memory capacitor 128. The composition of the thin film 124 of layered superlattice material is discussed in more detail below.

An electrically-conductive diffusion barrier layer 130 is deposited on top electrode layer 126. Diffusion barrier layer 130 has a thickness in the range of 20 to 200 nm, preferably in the range of 20 to 50 nm. In accordance with the invention, diffusion barrier layer 130 comprises iridium oxide. Layers 118, 122, 124, 126 and 130 are patterned, in as few as two patterning process steps, to form memory capacitor 128 with self-aligned diffusion barrier layer 130.

A second interlayer dielectric layer (ILD) 136 made of NSG (nondoped silicate glass) is deposited to cover ILD 116, ferroelectric memory capacitor 128 and diffusion barrier layer 130. A PSG (phospho-silicate glass) film or a BPSG film could also be used in layer 136.

ILD 136 is patterned to form wiring holes for electrical contacts to MOSFET 114 and ferroelectric memory capacitor 128. Wiring hole 142 is selectively opened through ILD 136 and ILD 116 to expose the source region 106, and wiring hole 144 is selectively opened through ILD 136 and ILD 116 to expose the gate region 108. Wiring hole 146 is selectively opened through ILD 136 to expose a portion of the bottom electrode 122. Wiring hole 148 is selectively opened through ILD 136 to expose diffusion barrier layer 130.

Source electrode metallized wiring layer 152 (also referred to as local interconnect or LI 152) and drain electrode metallized wiring layer 154 (also referred to as local interconnect or LI 154) are formed to fill wiring holes 142 and 144, respectively. Bottom electrode metallized wiring layer 156 (also referred to as local interconnect or LI 156) and top electrode metallized wiring layer 158 (also referred to as local interconnect or LI 158) are formed to fill wiring holes 146 and 148, respectively. The drain electrode metallized wiring layer 154 is electrically connected to bottom electrode metallized wiring layer 156, and preferably is the same wiring element. Each of these metallized wiring layers 152, 154, 156 and 158 preferably comprises Al-Si-Cu-Ti with a thickness of 200-300 nm.

In an alternative embodiment, as shown in FIG. 2, ILD 136 of memory cell 200 is formed on top electrode layer 126, and a wiring hole 248 is etched through ILD 136 down to top electrode layer 126. Then a diffusion barrier layer 230 is formed in wiring hole 248 prior to forming LI 158.

In a third exemplary embodiment depicted in FIG. 3, a memory capacitor 328 is "stacked" above the switch, namely MOSFET 314, of memory cell 300. A field oxide region 304 is formed on a surface of a silicon substrate 302. A source region 306 and a drain region 308 are formed separately from each other within silicon substrate 302. A gate insulating layer 310 is formed on silicon substrate 304 between the source and drain regions 306 and 308. Further, a gate electrode 312 is formed on the gate insulating layer 310. These source region 306, drain region 308, gate insulating layer 310 and gate electrode 312 together form a MOSFET 314.

A first interlayer dielectric layer (ILD) 316 made of BPSG (boron-doped phospho-silicate glass) is formed on substrate 304 and field oxide region 302. ILD 316 is patterned to form vias 315, 317 to source region 306 and drain region 308, respectively. Vias 315, 317 are filled to form electrically conductive plugs 318, 319, respectively. Conductive plugs 318, 319 typically comprise tungsten or polycrystalline silicon. A layer of iridium oxide is deposited on ILD 316 above plugs 318, 319 and MOSFET 314. The layer of iridium oxide is patterned and etched to form diffusion barrier layer 320 above conductive plug 318 (also referred to as local interconnect or LI 318) and source region 306, and diffusion barrier layer 321 above conductive plug 319 (also referred to as local interconnect or LI 319) and gate region 308. Diffusion barrier layer 320 is in electrical contact with conductive plug 318. Diffusion barrier

layer 321 is in electrical contact with conductive plug 319. The diffusion barrier layers typically have a thickness of 20 to 200 nm, preferably 20 to 50 nm.

As depicted in FIG. 3, a bottom electrode layer 322 made of platinum and having a thickness of 200 nm is deposited on diffusion barrier layer 321. Then a dielectric thin film 324 of ferroelectric layered superlattice material is formed on bottom electrode layer 322. Thin film 324 typically has a thickness in the range of 50-300 nm. A top electrode layer 326, made of platinum and having a thickness of 200 nm, is formed on the dielectric thin film 324. Bottom electrode layer 322, dielectric thin film 324 and top electrode layer 326 together form ferroelectric memory capacitor 328. The composition of dielectric thin film 324 is discussed in more detail below. Diffusion barrier layers 320, 321 inhibit the diffusion of chemical species contained in the local interconnects represented by conductive plugs 318, 319 to the region of the ferroelectric memory capacitor 328.

Wafer substrate 102, 302 may comprise silicon, gallium arsenide or other semiconductor, or an insulator, such as silicon dioxide, glass or magnesium oxide (MgO). The bottom and top electrodes of memory capacitors conventionally contain platinum. It is preferable that the bottom electrode contains a non-oxidized precious metal such as platinum, palladium, silver, and gold. In addition to the precious metal, metal such as aluminum, aluminum alloy, aluminum silicon, aluminum nickel, nickel alloy, copper alloy, and aluminum copper may be used for electrodes of a ferroelectric memory. Adhesive layers (not shown), such as titanium, enhance the adhesion of the electrodes to adjacent underlying or overlying layers of the circuits.

A second interlayer dielectric layer (ILD) 336 made of NSG (nondoped silicate glass) is deposited to cover ILD 316, diffusion barrier layers 320, 321, and ferroelectric memory capacitor 328. A PSG (phospho-silicate glass) film or a BPSG (boron phospho-silicate glass) film could also be used in layer 336.

ILD 336 is patterned to form a via 337 to diffusion barrier layer 320. A metallized wiring film is deposited to cover ILD 336 and fill via 337 and then patterned to form plug 337, source electrode metallized wiring layer 338, and top electrode metallized wiring layer 339, or local interconnect 339. Alternatively, a layer of iridium oxide may be deposited, patterned and etched to form diffusion barrier layer 329 before the wiring film is deposited. Metallized wiring layers 338, 339 preferably comprise Al-Si-Cu-Ti standard interconnect metal with a thickness of about

200-300 nm.

The word "substrate" can mean the underlying wafer 102, 302 on which the integrated circuit is formed, as well as any object on which a thin film layer is deposited, such as BPSG layer 116. In this disclosure, "substrate" shall mean the object to which the layer of interest is applied; for example, when we are talking about a bottom electrode, such as 122, the substrate includes the layers 118 and 116 on which the electrode 122 is formed.

Terms of orientation herein, such as "above", "top", "upper", "below", "bottom", and "lower" mean relative to the silicon substrate 102. That is, if a second element is "above" a first element, it means it is farther from the substrate 102, and if it is "below" another element then it is closer to the substrate 102 than the other element. The long dimension of substrates 102, 302 defines a plane that is considered to be a "horizontal" plane herein, and directions perpendicular to this plane are considered to be "vertical".

A memory cell typically comprises a relatively flat thin film of dielectric material. The terms "lateral" or "laterally" refer to the direction of the flat plane of the thin film. In FIG. 1, the lateral direction would be the horizontal direction.

This specification refers to a diffusion barrier layer located between a local interconnect and a thin film of layered superlattice material. The term "between" does not mean that the barrier layer is in direct contact with the thin film of layered superlattice material. Typically, the barrier layer does not contact the thin film of layered superlattice material; but the diffusion barrier layer typically is in direct contact with the local interconnect to prevent diffusion of titanium and other chemical species therefrom into other elements and regions of the integrated circuit. The term "on" is often used in the specification when referring to the deposition or formation of an integrated circuit layer onto an underlying substrate or layer. In contrast to "between", the term "on" generally signifies direct contact, as is clear in the various contexts in which it is used.

In the preferred embodiment of the invention, as depicted in FIG. 1, the diffusion barrier layer 130 is located above top electrode layer 126, directly over thin film 124 of layered superlattice material. Since the composition of the diffusion barrier layer according to the invention is electrically conductive, the diffusion barrier layer is not in direct contact with the sides of memory capacitor 128.

The term "thin film" is used herein as it is used in the integrated circuit art. Generally, it means a film of less than a micron in thickness. The thin films disclosed herein are in all instances less than 0.5 microns in thickness. Preferably, the iridium-oxide diffusion barrier layers of the invention are in the range of 20-50 nm. Preferably, the dielectric thin films 124, 324 are 50 nm to 300 nm thick, and most preferably 50 to 150 nm thick. These thin films of the integrated circuit art should not be confused with the layered capacitors of the macroscopic capacitor art which are formed by a wholly different process which is incompatible with the integrated circuit art.

The composition of the dielectric thin films 124, 324 can be selected from a group of suitable ferroelectric layered superlattice materials. Alternatively, the thin film 124, 324 may comprise nonferroelectric, high-dielectric constant layered superlattice materials used in DRAM cells

United States Patent No. 5,519,234 issued May 21, 1996 discloses that layered superlattice compounds, such as strontium bismuth tantalate (SBT), have excellent properties in ferroelectric applications as compared to the best prior materials and have high dielectric constants and low leakage currents. United States Patents Nos. 5,434,102 issued July 18, 1995 and 5,468,684 issued November 21, 1995, describe processes for integrating these materials into practical integrated circuits. Ferroelectric layered superlattice materials, like the metal oxides $SrBi_2Ta_2O_9$ (SBT) and $SrBi_2(Ta_{1-x}Nb_x)_2O_9$ (SBTN), where $0 \leq x \leq 1$, are currently under development for use as capacitor dielectrics in nonvolatile memory applications (FeRAM).

The layered superlattice materials may be summarized generally under the formula:

(1)
$$A1_{w1}^{+a1}A2_{w2}^{+a2}\ldots Aj_{wj}^{+aj}S1_{x1}^{+s1}S2_{x2}^{+s2}\ldots Sk_{sk}^{+sk}B1_{y1}^{+b1}B2_{y2}^{+b2}\ldots Bl_{yl}^{+bl}Q_{z}^{-2},$$

where A1, A2...Aj represent A-site elements in the perovskite-like structure, which may be elements such as strontium, calcium, barium, bismuth, lead, and others; S1, S2...Sk represent superlattice generator elements, which usually is bismuth, but can also be materials such as yttrium, scandium, lanthanum, antimony, chromium, thallium, and other elements with a valence of +3; B1, B2...Bl represent B-site elements in the perovskite-like structure, which may be elements such as titanium,

tantalum, hafnium, tungsten, niobium, zirconium, and other elements; and Q represents an anion, which generally is oxygen but may also be other elements, such as fluorine, chlorine and hybrids of these elements, such as the oxyfluorides, the oxychlorides, etc. The superscripts in formula (1) indicate the valences of the respective elements, and the subscripts indicate the number of moles of the material in a mole of the compound, or in terms of the unit cell, the number of atoms of the element, on the average, in the unit cell. The subscripts can be integer or fractional. That is, formula (1) includes the cases where the unit cell may vary throughout the material; e.g. in $SrBi_2(Ta_{0.75}N_{0.25})_2O_9$, on the average, 75% of the B-sites are occupied by a tantalum atom and 25% of the B-sites are occupied by a niobium atom. If there is only one A-site element in the compound, then it is represented by the "A1" element and w2...wj all equal zero. If there is only one B-site element in the compound, then it is represented by the "B1" element, and y2...yl all equal zero, and similarly for the superlattice generator elements. The usual case is that there is one A-site element, one superlattice generator element, and one or two B-site elements, although formula (1) is written in the more general form since the invention is intended to include the cases where either of the sites and the superlattice generator can have multiple elements. The value of z is found from the equation:

(2) $(a1w1 + a2w2...+ajwj) + (s1x1 + s2x2...+skxk) + (b1y1 +b2y2...+ blyl) = 2z.$

Formula (1) includes all three of the Smolenskii type compounds discussed in United States Patent No. 5,519,234 issued May 21, 1996. The layered superlattice materials do not include every material that can be fit into Formula (1), but only those which spontaneously form themselves into crystalline structures with distinct alternating layers.

The terms "layered superlattice material", "layered superlattice compound", and "layered superlattice material compound" are used virtually interchangeably in this specification and their meaning is clear from the context.

It is known in the art that ferroelectric nonvolatile memories possessing good electronic properties are fabricated by forming a thin film of strontium bismuth tantalate material comprising chemical elements in proportions approximately represented by the stoichiometric formula $SrBi_2Ta_2O_9$. Based on the Watanabe et al.

5,434,102 patent and related work, the precursor for making layered superlattice materials currently preferred by those skilled in the art has the stoichiometric formula $SrBi_{2.18}Ta_{1.44}Nb_{0.56}O_9$.

2. *Detailed Description of the Fabrication Process*

The diagram of FIG. 4 is a flow sheet of the fabrication process 410 to make a ferroelectric memory 100 incorporating a diffusion barrier layer 130 in a preferred embodiment of the invention, according to FIG. 1. The ferroelectric memory 100 is preferably formed on a conventional wafer that may be silicon, gallium arsenide or other semiconductor, or an insulator, such as glass or magnesium oxide (MgO). In step 412, a semiconductor substrate 102 (FIG. 1) is provided on which a switch 114 is formed in step 414. The switch is typically a MOSFET. In step 416, a first interlayer dielectric (ILD) layer 116 is formed to separate the switching element from the ferroelectric element to be formed. In step 418, a bottom electrode layer 122 is formed. Preferably, the electrode layer 122 is made of platinum and is sputter-deposited to form a layer with a thickness of about 200 nm. In the preferred method, an adhesion layer 118 made of titanium or titanium nitride of about 20 nm would be formed in this step, preferably by sputtering, prior to depositing the electrode. In step 420, chemical precursors of the desired thin film of layered superlattice material are prepared. Preferably, the precursors contain compounds for forming ferroelectric layered superlattice materials having the stoichiometric formula $SrBi_{2.18}Ta_{1.44}Nb_{0.56}O_9$. The precursor is applied to the bottom electrode layer 122 in step 422. A MOCVD method is the most preferred method to form the dielectric thin film. The precursor also can be applied using a liquid deposition technique, such as a spin-coating or a misted deposition method as described in United States Patent No. 5,456,945. Usually, a final precursor solution is prepared from commercially available solutions containing the chemical precursor compounds. Preferably, the concentrations of the various precursors supplied in the commercial solutions are adjusted in step 420 to accommodate particular manufacturing or operating conditions. For example, the stoichiometric amounts of the various elements in a typical commercial solution for a layered superlattice thin film might be $SrBi_{2.18}Ta_{1.44}Nb_{0.56}O_9$. It is often desirable, however, to add extra niobium or bismuth to this solution to generate extra oxides that will protect the ferroelectric compounds from hydrogen degradation during reducing conditions. The application step 422 is preferably followed by a treatment process

424, which typically includes drying and heating at elevated temperatures, such as in a hot-plate bake and a rapid thermal process (RTP) anneal; treatment step 424 may include treatment with ultraviolet radiation during or after the application step 422. Steps 422 and 424 may be repeated (indicated by the dashed line in FIG. 4) as necessary to form a film of the desired thickness. For example, in a typical spin-on procedure, a coat of the precursor might be applied, dried and RTP-treated. Then another precursor coat might be applied, dried and RTP-treated. Typically, in step 426 the coating is then annealed in oxygen to form the dielectric thin film 124 with desired properties. Following steps 422-426, the top electrode layer 126 is formed in step 428. Preferably, top electrode layer 126 is made of platinum and is sputter-deposited to form a layer with a thickness of about 200 nm. In step 430, diffusion barrier layer 130 is deposited. Diffusion barrier layer 130 comprises iridium oxide, IrO_2. Preferably, diffusion barrier layer 130 is deposited on top electrode layer 126 by a sputtering process. Preferably, it has a thickness of about 20-50 nm.

Patterning steps via processes such as ion milling and ashing, as known in the art, are also included as appropriate in the fabrication of memory cell 100. For example, step 418 may include such a patterning process, and another patterning process may follow step 426. Preferably, however, a plurality of layers are patterned in a single patterning step. Barrier layer formation step 430 preferably includes a patterning and etching process in which the stacked layers 118, 122, 124, 126 and 130 are patterned to form ferroelectric memory capacitor 128, covered by self-aligning diffusion barrier layer 130. Preferably, only two etching processes are required to complete the patterning processes of step 430. Preferably, a conventional ion milling process is used. A second ILD layer 136 is deposited in step 432 to cover ILD 116 and memory capacitor 128, including diffusion barrier layer 130. In step 434, wiring holes 142, 144, 146, and 148 are made through the ILD layers 116 and 136, as depicted in FIG. 1, to the switch 114 (typically to the source and drain regions of a MOSFET), to the bottom electrode 122, and to diffusion barrier layer 130, respectively. Preferably, a standard ion milling process forms wiring holes 142, 144, 146, and 148. Thereafter, metallized wiring layers ("LI") 152, 154, 156, and 158 are formed, as depicted in FIG. 1, preferably using a sputtering process. LI 152, 154, 156 and 158 are patterned and etched using conventional processes, and then annealed at about 450°C.

The circuit is completed in step 336, which typically includes deposition of a passivation layer.

FIG. 5 is a top view of an exemplary wafer on which thin film capacitors 596, 598 and 600 fabricated on wafer 500 in accordance with the invention are shown greatly enlarged. FIG. 6 is a portion of a cross-section of FIG. 5 taken through the lines 6-6, illustrating a thin film capacitor device fabricated in accordance with the invention. A silicon dioxide layer 604 is formed on a silicon crystal substrate 602. Then bottom electrode 622 made of platinum is sputter-deposited on silicon dioxide layer 604. Layer 624 is a thin film of ferroelectric layered superlattice material, and layer 626 represents the top electrode made of platinum. A diffusion barrier layer 630 comprising iridium oxide is located on top electrode 626, and an ILD 636 is formed on layer 630. A wiring hole 648 is etched in layer 636, and titanium-containing LI metallization layer 658 is formed to fill wiring hole 648 and make contact with electrically conductive diffusion barrier layer 630.

EXAMPLE 1

The electronic properties of strontium bismuth tantalate capacitors were measured to study the efficacy of iridium oxide (IrO_2) as a barrier layer in protecting against diffusion of titanium from a titanium-containing local interconnect into the ferroelectric thin film.

The capacitors were fabricated from a strontium bismuth tantalate (SBT) precursor solution commercially available from the Kojundo Chemical Corporation. The solution contained amounts of chemical precursors corresponding to the stoichiometric formula $SrBi_2Ta_2O_9$. The 0.2 mol/l precursor commercial solution contained: bismuth 2-ethylhexanoate, strontium 2-ethylhexanoate, and tantalum 2-ethylhexanoate. Ferroelectric capacitors containing the layered superlattice compound were formed from the precursor solution in general accordance with the method described in Watanabe, U.S. Patent No. 5,434,102.

A series of p-type 100 Si wafer substrates 602 were oxidized to form a layer of silicon dioxide 604. These were dehydrated 30 minutes at 180°C in a low vacuum. Then a bottom platinum electrode 622 with a thickness of 200 nm was sputter-deposited on silicon dioxide layer 604, annealed 30 minutes in O_2 at 650°C., and dehydrated as above. The 0.2 molar SBT-precursor solution was diluted with n-butyl acetate to 0.12 molar concentration prior to deposition. A spincoat of the 0.12 molar

solution of the SBT-precursor was deposited on the bottom electrode 622 at 1500 rpm for 30 seconds. This was dehydrated by a hot-plate bake at 160°C for one minute, and at 260°C for four minutes; then a RTP was conducted in oxygen at 725°C for 30 seconds, with a ramping rate of 100°C per second. The sequence of the spincoat, baking and RTP steps was repeated. These steps formed a ferroelectric thin film 624 having a thickness of 180-190 nm. The wafer and deposited layers were given a so-called ferro-anneal for 60 minutes at 800°C in O_2 gas, with 10 minutes push/pull. Platinum was sputter-deposited to make a top electrode layer 626 with a thickness of 200 nm. On certain experimental wafers, a diffusion barrier layer 630 according to the invention was formed. An iridium target was sputtered using an argon atmosphere to form a layer of iridium with a thickness of 100 nm. In the ensuing oxygen anneal steps described below, the deposited iridium was oxidized to form a layer of iridium oxide in accordance with the invention. The layers 622, 624, and 626, as well as 630 when present, were patterned and etched using conventional methods to form capacitors, and then ashing was performed, followed by a first recovery anneal for 30 minutes at 800°C in O_2 gas flowing at 6 liters per minute, with 10 minutes push/pull. An ILD layer 636 was deposited on the wafer using a spin-on method. A layer of spin-on-glass ("SOG") was applied using 3000 rpm for 30 seconds. This was hot-plate baked at 160°C for five minutes, and at 260°C for five minutes, followed by an SOG anneal at 800°C for five minutes in oxygen gas flowing at 5 liters per minute, with five minutes push/pull. The sequence of spin-on, bake and anneal steps was repeated twice. The ILD 636 was patterned and etched using conventional methods, then a second recovery anneal was performed at 800°C for five minutes in oxygen gas flowing at 5 liters per minute, with 10 minutes push/pull.

Finally, LI ("local interconnect") layer 658 comprising principally platinum was formed either on top electrode layer 626, or on diffusion barrier layer 630, if present. On certain wafers, a titanium adhesion sublayer was deposited prior to depositing the platinum. The titanium adhesion sublayer was deposited by sputtering a titanium target at 8 mTorr pressure in an argon atmosphere. The platinum was deposited by sputtering a platinum target. Upon annealing, the titanium adhesion sublayer, if used, diffuses into the adjacent layers and is, therefore, not discernable as a distinct layer. After patterning and etching the LI layer 658, test anneals and measurements of electronic properties of the resulting capacitors were performed. These experimental

capacitors had a surface area of about 900 μm^2.

Thus, three types of test capacitors were formed and studied. In the first type, only platinum was deposited to form LI layer 658, so the capacitor contained no titanium in LI layer 658. In the second type, LI layer 658 was formed by depositing a titanium adhesion sublayer and then platinum on the platinum top electrode layer 626. Thus, titanium was present at the interface of top electrode layer 626 and LI layer 658. The first and second types did not have an inventive diffusion barrier layer. In the third type, diffusion barrier layer 630 comprising iridium oxide in accordance with the invention was formed on platinum top electrode layer 626, and then LI layer 658 comprising titanium and platinum was formed.

The surface area of contact between LI layer 658 and the underlying layer, either top electrode layer 626 or diffusion barrier layer 630, was varied. In one set of the three types of capacitor, the area of contact was about 90% of the surface area of the top electrode 626 of the capacitor. In a second set of the three types of capacitor, the area of contact was about 10% of the top electrode. It should be noted that the surface area of the experimental capacitors, 900 μm^2, was relatively large. In actual commercial integrated circuits, the surface areas are often only 100 μm^2. This means that an experimental LI layer contacting about 10% of the underlying experimental capacitor surface would contact virtually 100% of the top surface of a commercial capacitor having a surface area of 100 μm^2, thereby corresponding to a maximum surface area of potential titanium diffusion.

From hysteresis curves measured at 3 volts, the remnant polarization of the capacitors was calculated as the 2Pr-value, in units of $\mu C/cm^2$. Initial measurements were made after the LI layer 658 was deposited and etched, before annealing. Then the capacitors were annealed at 400°C for 30 minutes in oxygen-gas flowing at 5 liters per minute, with 10 minutes push/pull, and the 2Pr-values were measured again. The sequence of annealing and measuring was repeated at annealing temperatures of 450°C and 500°C.

The results of the experimental measurements are shown in the graph of FIG. 7. For each set of fabrication conditions, the measurements were conducted usually on five capacitors and averaged. Thus, each point plotted on the graph of FIG. 7 represents the average value from measurements of five test capacitors. In FIG. 7, the average 2Pr-value, in units of $\mu C/cm^2$, is plotted versus annealing conditions. The

experimental average values from Capacitors 1 are represented by the solid circles connected by the solid line. Capacitors 1 contained no diffusion barrier, and their LI layer contacted about 90% of the top electrode surface area of Capacitors 1. Capacitors 2, represented by upright triangles connected by a dotted line, had no diffusion barrier, but their LI layer covering 90% of their top electrode surface did include titanium. Capacitors 3, represented by solid squares connected by a dot-dash line, were covered by an iridium-oxide diffusion barrier, and their LI layer, covering 90% of their top electrode surface, included titanium. Capacitors 4, represented by solid diamonds connected by short dashes, had no diffusion barrier and no titanium in their LI, and the LI covered only 10% of their top electrode surface. Capacitors 5, represented by solid triangles connected by long dashes, had no diffusion barrier, but contained titanium in their LI, and the LI covered 10% of their top electrode surface. Capacitors 6, represented by empty circles connected by a dot-dash line, had both an iridium-oxide diffusion barrier and titanium in their LI, and the LI covered 10% of their top electrode surface.

The data plotted in FIG. 6 show that, before annealing of the LI layer, the average 2Pr-value in the various capacitors was in the range of about 12.5 to 14.5 $\mu C/cm^2$. After annealing at 400°C, however, the 2Pr-value in Capacitors 2, having no diffusion barrier, but having titanium in the LI layer, and having 90% of their surface area covered by the LI, dropped precipitously to about 8.5 $\mu C/cm^2$. This was presumably caused by diffusion of titanium through the platinum into the ferroelectric material. In contrast, the 2Pr-value of Capacitors 1, which had no titanium, stayed about the same after annealing at 400°C, as did the 2Pr-value of Capacitors 3, which contained titanium in their LI, but which were protected by the iridium-oxide diffusion barrier, in accordance with the invention. The 2Pr-values in Capacitors 4 and 6 remained essentially unchanged after annealing at 400°C. The 2Pr-value in Capacitors 5 actually increased after annealing at 400°C, even though Capacitors 5 contained titanium in their LI and were not protected by an iridium-oxide layer. This can be explained by the fact that only 10% of the total top electrode surface area of Capacitors 5 was in contact with the titanium-containing LI, so the relative amount of diffusing titanium was insignificant, and the improvement in electrical contact between LI and capacitor caused by annealing was the dominant effect.

After annealing at 450°C and 500°C, the average 2Pr-value in Capacitors 1,

3-6 was basically unchanged. In Capacitors 2, however, the polarizability after additional annealing was so low that the 2Pr-value could not be measured. The experimental results depicted in FIG. 7 show that the iridium oxide diffusion barrier of the invention effectively protects layered superlattice material by inhibiting diffusion of chemical species from a LI layer into the layered superlattice material.

There has been described structures and fabrication methods of a novel composition of diffusion barrier layer for protecting layered superlattice materials in integrated circuits. The diffusion barrier layer of the invention protects layered superlattice material by inhibiting diffusion of chemical species from LI layers. In particular, there has been described a composition, a structure and a method for fabricating an integrated circuit containing layered superlattice material in a memory capacitor that permits the use of standard LI layers and still results in devices with good electronic properties. It should be understood that the particular embodiments shown in the drawings and described within this specification are for purposes of example and should not be construed to limit the invention which will be described in the claims below. Further, it is evident that those skilled in the art may now make numerous uses and modifications of the specific embodiments described, without departing from the inventive concepts. It is also evident that the steps recited may in some instances be performed in a different order; or equivalent structures and processes may be substituted for the various structures and processes described.

WE CLAIM:

1. An integrated circuit comprising: a thin film (124, 324, 624) of layered superlattice material; and a local interconnect (158, 318, 319, 339, 658); said integrated circuit characterized by a diffusion barrier layer (130, 136, 329, 320, 321, 630), said diffusion barrier layer comprising iridium oxide and located between said thin film of layered superlattice material and said local interconnect to inhibit diffusion of a chemical species from said local interconnect towards said thin film of layered superlattice material.

2. An integrated circuit as in claim 1, characterized in that said local interconnect is a metallized wiring layer (158, 339, 658), and said thin film of layered superlattice material is a dielectric thin film in a memory capacitor (128, 328, 600).

3. An integrated circuit as in claim 2, further characterized by a top electrode layer (126, 326, 626) located on said dielectric thin film, and wherein said diffusion barrier layer is located above said top electrode layer, and said metallized wiring layer is located above said diffusion barrier layer.

4. An integrated circuit as in claim 1, characterized in that said local interconnect is an electrically conductive plug (318, 319), said thin film of layered superlattice material is a dielectric thin film in a memory capacitor (324), and said memory capacitor is above said electrically conductive plug.

5. An integrated circuit as in claim 4, characterized in that said memory capacitor comprises a bottom electrode layer (122, 322, 622), said dielectric thin film is located on said bottom electrode layer, said diffusion barrier layer is above said electrically conductive plug, and said bottom electrode layer is above said diffusion barrier layer.

6. An integrated circuit as in claim 1 characterized in that said chemical species is a metal.

7. An integrated circuit as in claims 1, 2, 3, 4 or 5, characterized in that said chemical species is a material selected from the group consisting of tungsten, titanium, titanium nitride, aluminum, copper and silicon.

8. An integrated circuit as in claim 1, 2, 3, 4, 5, or 6 characterized in that said diffusion barrier layer is in direct contact with said local interconnect.

9. An integrated circuit as in claim 1, 2, 3, 4, 5, or 6, characterized in that said dielectric thin film comprises nonferroelectric, high-dielectric constant material.

10. An integrated circuit as in claim 9 characterized in that said diffusion barrier layer is in direct contact with said local interconnect.

11. An integrated circuit as in claim 1, 2, 3, 4, 5 or 6, characterized in that said dielectric thin film comprises ferroelectric material.

12. An integrated circuit as in claim 11, characterized in that said ferroelectric material comprises at least three materials selected from the group consisting of strontium, bismuth tantalum and niobium.

13. An integrated circuit as in claim 11 characterized in that said diffusion barrier layer is in direct contact with said local interconnect.

14. A method of forming an integrated circuit comprising steps of forming a thin film (124, 324, 624) of layered superlattice material, and forming a local interconnect (158, 318, 319, 339, 658); said method characterized by the step of forming a diffusion barrier layer (130, 136, 329, 320, 321, 630), said diffusion barrier layer comprising iridium oxide and located between said thin film of layered superlattice material and said local interconnect to inhibit diffusion of a chemical species from said local interconnect towards said thin film of layered superlattice material.

15. A method of forming an integrated circuit as in claim 14, characterized in that said local interconnect is a metallized wiring layer (158, 339, 658), and said thin film of layered superlattice material is a dielectric thin film in a memory capacitor (128, 328, 600).

16. A method of forming an integrated circuit as in claim 15, further characterized by a step of forming a top electrode layer (126, 326, 626) on said dielectric thin film, characterized in that said diffusion barrier layer is formed above said top electrode layer, and said metallized wiring layer is formed above said diffusion barrier layer.

17. A method of forming an integrated circuit as in claim 14, characterized in that said local interconnect is an electrically conductive plug (318, 319), and said thin film of layered superlattice material is a dielectric thin film in a memory capacitor (324).

18. A method of forming an integrated circuit as in claim 17, characterized in that said diffusion barrier layer is formed above said electrically conductive plug, and further comprising a step of forming a bottom electrode layer (122, 322, 622) above said diffusion barrier layer, and characterized in that said dielectric thin film is formed on said bottom electrode layer.

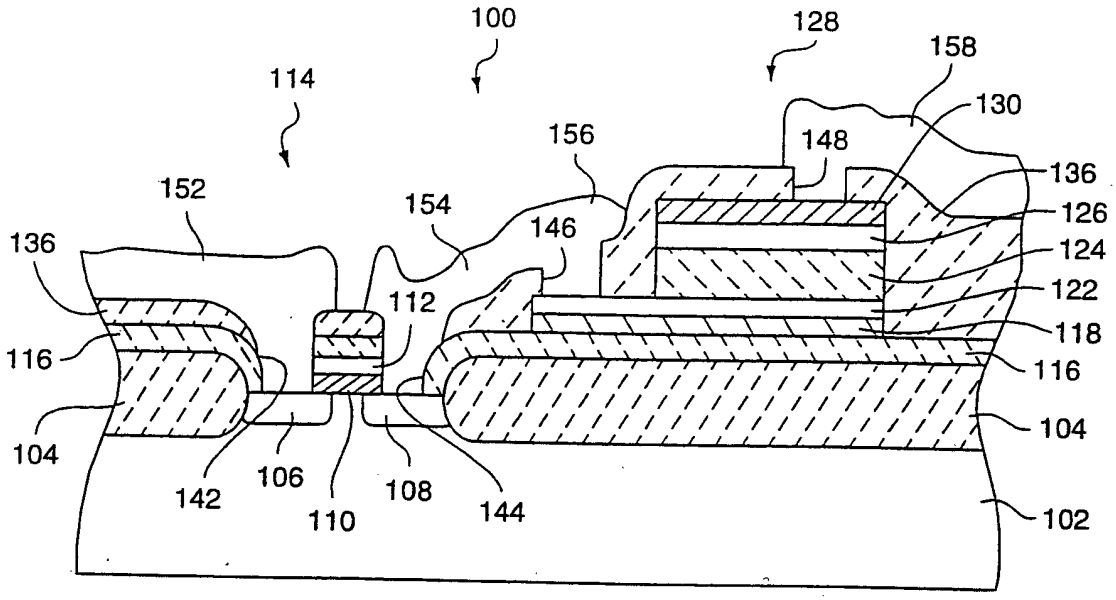
19. A method of forming an integrated circuit as in claim 14, 15, 16, 17 or 18, characterized in that said step of forming a diffusion barrier lay r comprises forming said diffusion barrier layer in direct contact with said local interconnect.

20. A method of forming an integrated circuit as in claim 14, 15, 16, 17 or 18 characterized in that said dielectric thin film comprises nonferroelectric, high-dielectric constant material.

21. A method of forming an integrated circuit as in claim 20 characterized in that said step of forming a diffusion barrier layer comprises forming said diffusion barrier layer in direct contact with said local interconnect.

22. A method of forming an integrated circuit as in claim 14, 15, 16, 17, or 18 characterized in that said dielectric thin film comprises ferroelectric material.

23. A method of forming an integrated circuit as in claim 22 characterized in that said step of forming a diffusion barrier layer comprises forming said diffusion barrier layer in direct contact with said local interconnect.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142
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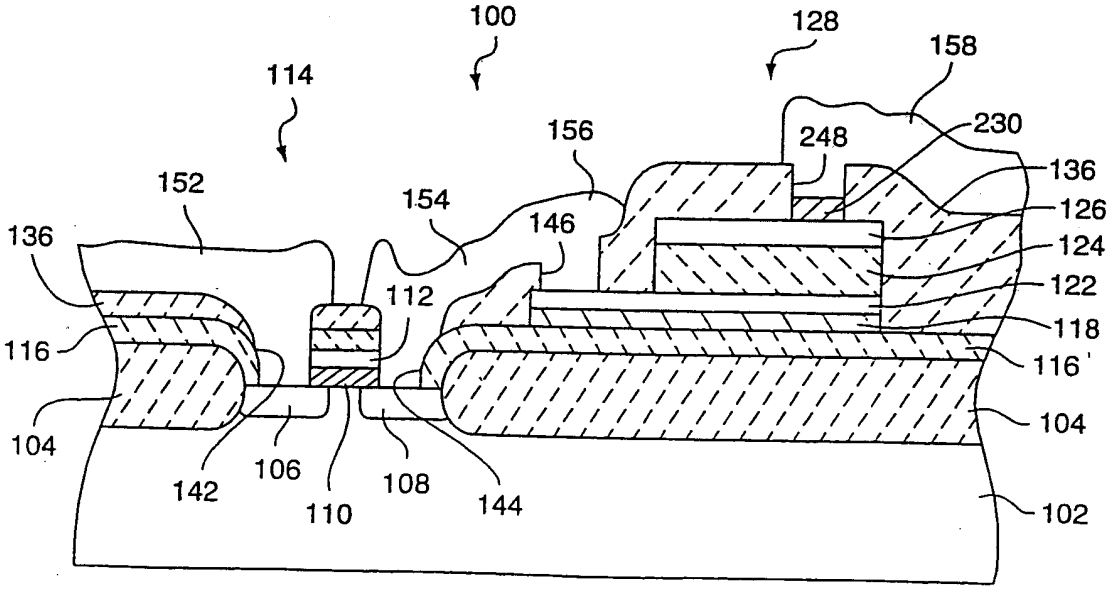
144
102

FIG. 1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152
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142
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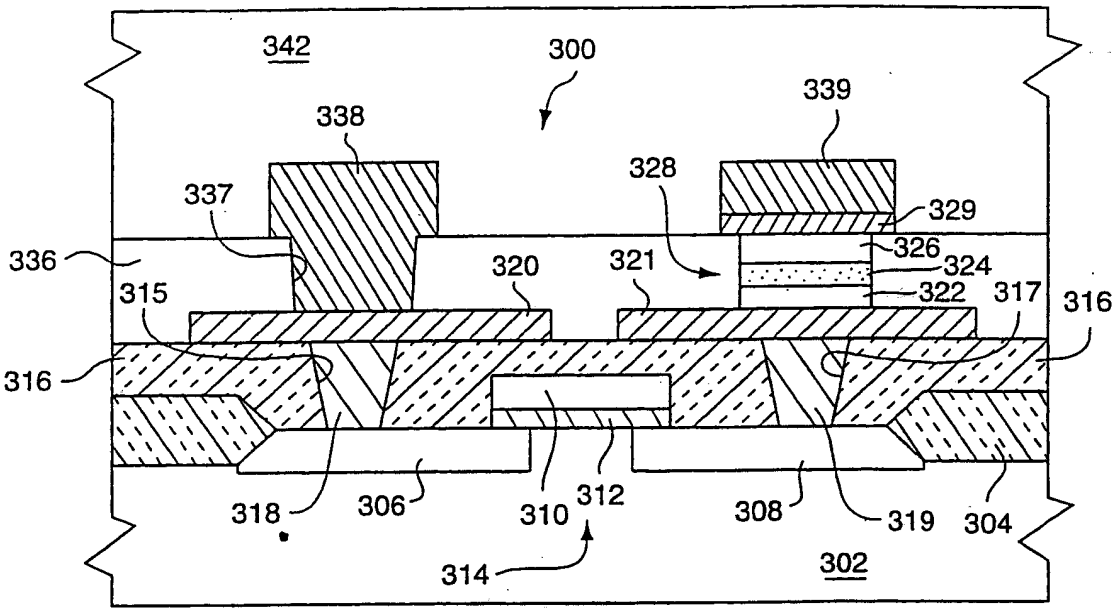
110
144
102

FIG. 2


342
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339
338
328
337
329
336
326
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324
315
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316
316
318
306
310
312
308
319
304
314
302

FIG. 3

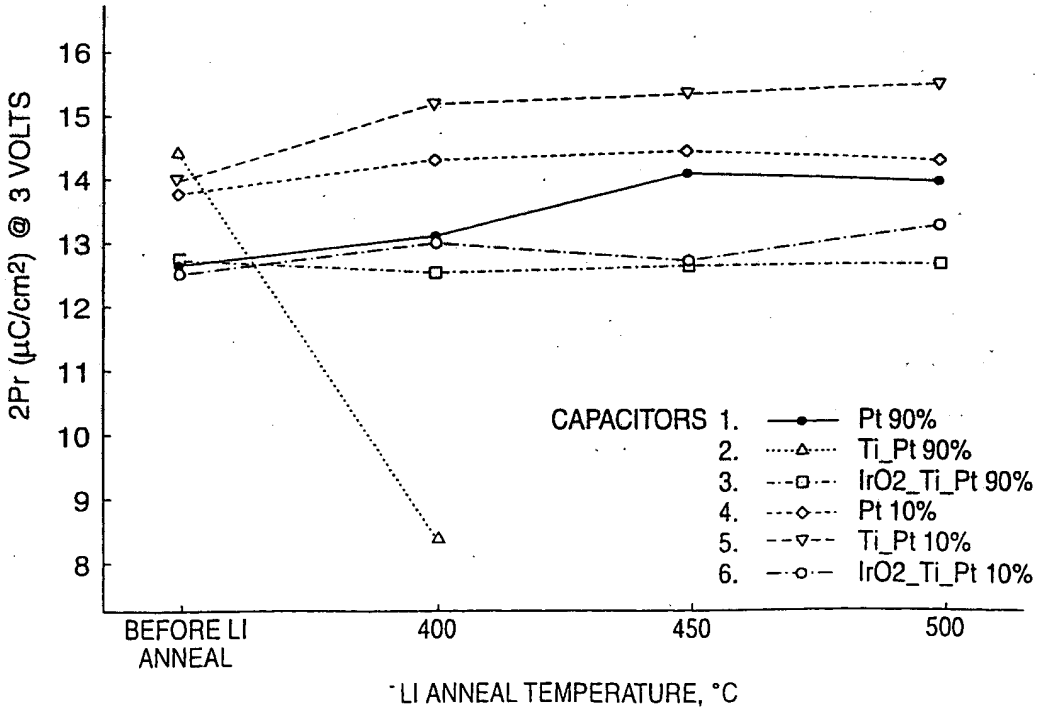
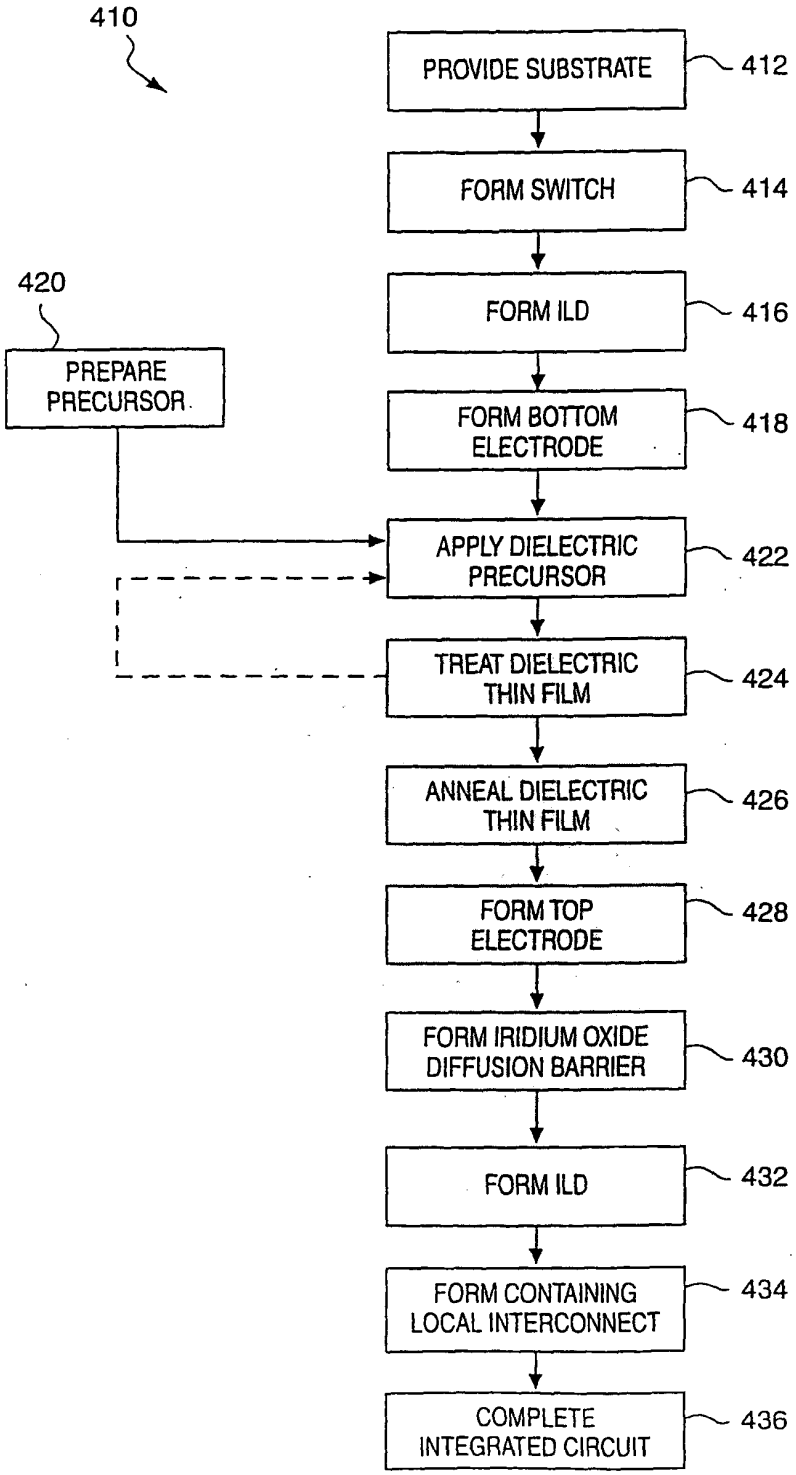

2Pr (μC/cm2) @ 3 VOLTS
16
15
14
13
12
11
10
9
8
BEFORE LI ANNEAL
400
450
500
LI ANNEAL TEMPERATURE, °C
CAPACITORS 1. Pt 90%
2. Ti_Pt 90%
3. IrO2_Ti_Pt 90%
4. Pt 10%
5. Ti_Pt 10%
6. IrO2_Ti_Pt 10%

FIG. 7

FIG. 4


410
PROVIDE SUBSTRATE
412
FORM SWITCH
414
FORM ILD
416
FORM BOTTOM ELECTRODE
418
420
PREPARE PRECURSOR
APPLY DIELECTRIC PRECURSOR
422
TREAT DIELECTRIC THIN FILM
424
ANNEAL DIELECTRIC THIN FILM
426
FORM TOP ELECTRODE
428
FORM IRIDIUM OXIDE DIFFUSION BARRIER
430
FORM ILD
432
FORM CONTAINING LOCAL INTERCONNECT
434
COMPLETE INTEGRATED CIRCUIT
436

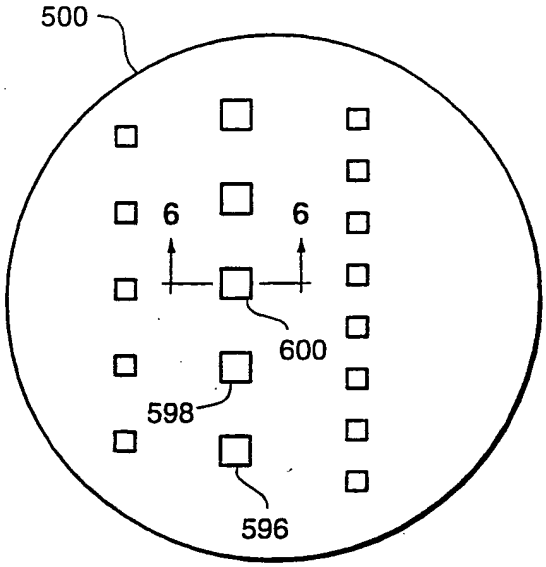


FIG. 5

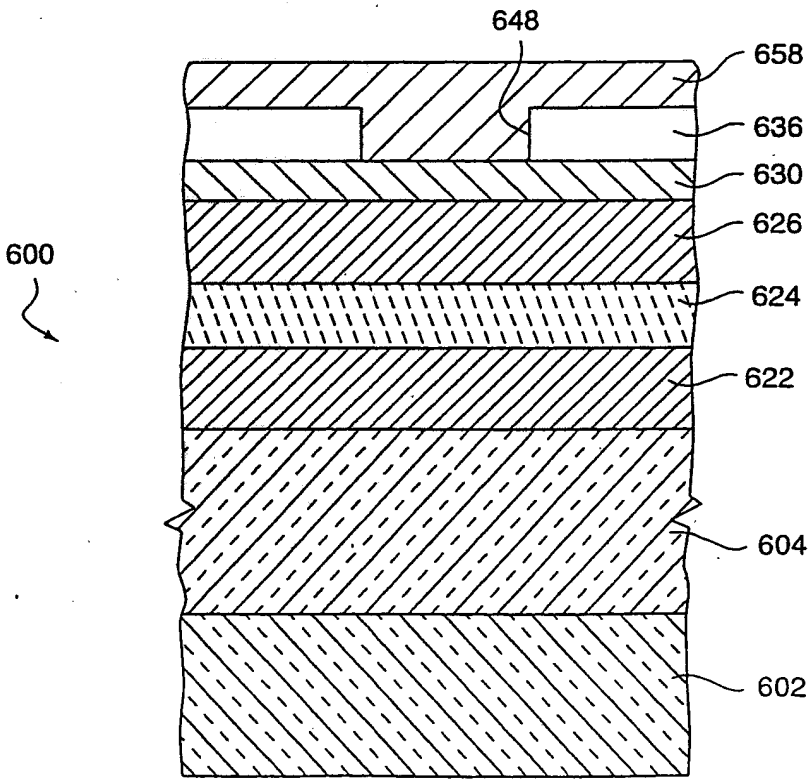


FIG. 6

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/03690

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/115 H01L21/02 H01L21/8242

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 886 317 A (SANYO ELECTRIC CO) 23 December 1998 (1998-12-23)	1,2,4, 6-8, 10-15, 17,19, 21-23
Y	the whole document	3,5,16, 18
Y	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 11, 30 September 1998 (1998-09-30) & JP 10 173138 A (FUJITSU LTD), 26 June 1998 (1998-06-26) abstract; figure 13	3,16

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 June 2000	16/06/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Blackley, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 00/03690

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
Y	CHO H -J ET AL: "PREPARATION AND CHARACTERIZATION OF IRIDIUMOXIDE THIN FILMS GROWN BY DC REACTIVE SPUTTERING" JAPANESE JOURNAL OF APPLIED PHYSICS,JP,PUBLICATION OFFICE JAPANESE JOURNAL OF APPLIED PHYSICS. TOKYO, vol. 36, no. 3B, PART 01, 1 March 1997 (1997-03-01), pages 1722-1727, XP000703099 ISSN: 0021-4922 the whole document	5,18
X	IZUMI N ET AL: "PROPERTIES OF FERROELECTRIC MEMORY WITH IR SYSTEM MATERIALS AS ELECTRODES" IEICE TRANSACTIONS ON ELECTRONICS,JP,INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, vol. E81-C, no. 4, April 1998 (1998-04), pages 513-516, XP000833776 ISSN: 0916-8524 the whole document	1

INTERNATIONAL SEARCH REPORT

...ormation on patent family members

Inter nal Application No
PCT/US 00/03690

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0886317 A	23-12-1998	JP 11008356 A	12-01-1999
JP 10173138 A	26-06-1998	US 5905278 A	18-05-1999

Docket # MUH-12757

Applic. #_____

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